

Low-power Wake-up Receiver With Subthreshold CMOS Circuits for Wireless Sensor Networks

Kazuhiro Takahagi[†], Hiromichi Matsushita*, Tomoki Iida[†], Masayuki Ikebe*, Yoshihito Amemiya*, Eiichi Sano[†]

[†] Research Center for Integrated Quantum Electronics, Hokkaido University, Japan

* Graduate School of Information Science and Technology, Hokkaido University, Japan

Introduction

Sensor LSIs for wireless sensor networks

- Only limited power sources (micro-miniature batteries...etc.)
- Long-term operation

⇒ Reducing power consumption is required to develop wireless sensor LSIs

- Wake-up receiver introduced in sensor LSIs.

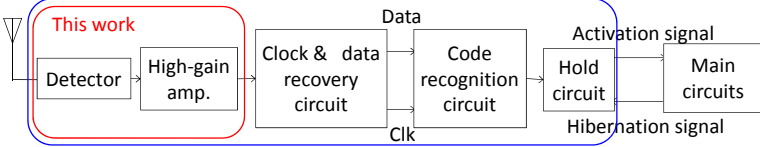
This work:

We propose low power wake-up receiver with CMOS technology operating in subthreshold current region.

Wake-up receiver

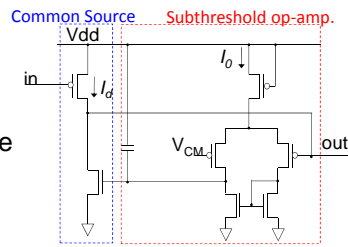
- Baseband signal: 10-100 kbps on-off keying (OOK)
- Carrier frequency: 2.4 GHz

Wake-up receiver



Direct-detector

- ✓ Achieve high-frequency carrier detection in subthreshold region
- ✓ p-MOS driver to decrease $1/f$ noise



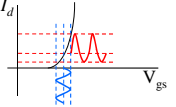
Instantaneous response

High-speed voltage response is difficult, but drain current responds instantaneously to input

Drain current $I_d = \frac{\beta v^2}{4}$

Nonlinearly

Characteristics of gate voltage – drain current (Square or exponential)



Subthreshold-operational amplifier

- ✓ Circuit topology is same as that of ordinary op-amp. However, very small tail current ($I_0 < 1$ nA)

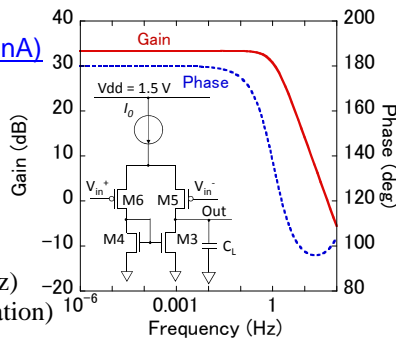
➢ 3-dB cut-off frequency

$$f_c = \frac{1}{2\pi(r_{o3} \parallel r_{o5})C_L} = 1.1 \text{ (Hz)}$$

➢ Unity-gain frequency

$$f_u = A_v \cdot f_c = \frac{I_0}{4\pi m_5 V_T C_L} = 50 \text{ (Hz)}$$

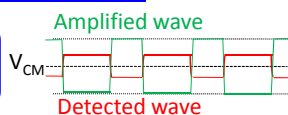
(Simulation)



High-gain amplifier

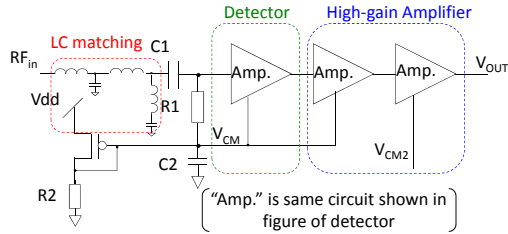
- ✓ Extremely high-gain amplifier (>100 dB) ⇒ DC offset problem
- ✓ Introduction of subthreshold op-amp. bias circuit

DC – very low frequency: No gain
AC (high frequency): Amplification



Detector and high-gain amp. design

- Used process: 1-poly. Si 6-metal 0.18μm CMOS process

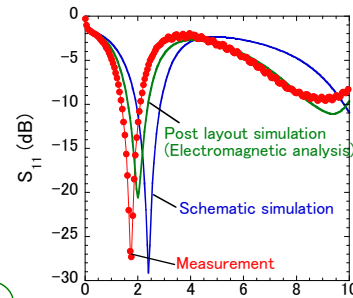


Size: 800 × 810 μm (without matching: 300 × 290 μm)

LC matching circuit

Matching frequency
(designed): 2.4 GHz
(fabrication): 1.75 GHz
(Caused by the wiring and pad)

- ✓ Measurements performed at carrier frequency of 1.75 GHz

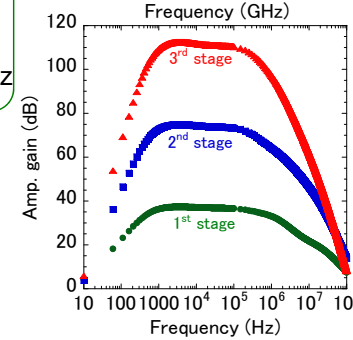
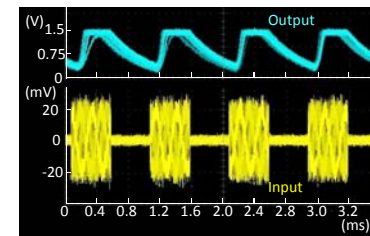


Design gain

- Gain/stage: 38 dB
- 3rd stage gain: 115 dB
- Frequency band: 1 k - 100 kHz

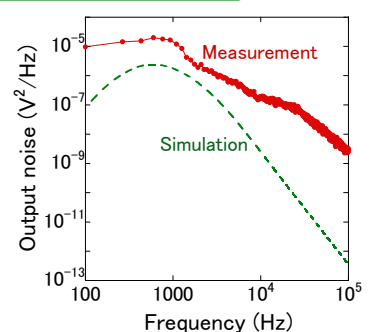
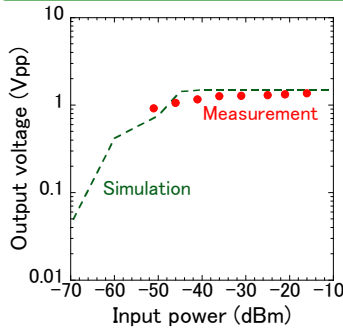
Measurement results

Oscilloscope wave form



Input power: -21 dBm
Baseband frequency: 1 kHz
Carrier frequency: 1.75 GHz
Common mode voltage: 0.75 V

Input-output and output noise characteristics



Sensitivity and power consumption

$$\text{Sensitivity} = \frac{3.5 \int N(f) df}{\gamma}$$

Bit-error-rate: 10^{-3} (assumed)
Signal-to-noise: 11dB (ASK)

Sensitivity (Measured): -47.2 dBm
(Simulated): -58.0 dBm

Power consumption (Measured): 6.8 μW
(Simulated): 7.0 μW

Future work

Reduce noise in detector to increase sensitivity